

What is claimed is:

1. ~~A computer system comprising:~~
a bus;
a processor; and
a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store instructions to implement microcode functions.
2. The computer system of claim 1 wherein the computer readable medium is firmware.
3. The computer system of claim 1 wherein the computer readable medium is a mass storage device.
4. The computer system of claim 1 wherein the instructions implement microcode functions by triggering processor hardware logic.
5. The computer system of claim 1 wherein the processor further comprises a plurality of registers associated with one or more functional units of the processor.
6. The computer system of claim 5 wherein the instructions implement microcode functions by updating one or more of the plurality of registers.
7. The computer system of claim 5 wherein the instructions implement microcode functions by reading one or more of the plurality of registers.
8. The computer system of claim 5 wherein the instructions implement microcode functions by triggering processor hardware logic and by manipulating the plurality of registers.

9. ~~A method comprising:~~
storing programmed code on a computer readable medium external to a processor;
executing, by the processor, the programmed code; and
controlling one or more functions of the processor in response to executing the
programmed code.

Sub Q1/ 10. ~~The method of claim 9 wherein the one or more functions are controlled by~~
directly triggering hardware on the processor in response to executing the programmed
code.

11. ~~The method of claim 9 wherein the one or more functions are controlled by~~
updating one or more registers associated with a logic unit on the processor in response to
executing the programmed code.

12. The method of claim 9 wherein the one or more functions are controlled by
triggering processor hardware logic and by manipulating the plurality of registers.

13. The method of claim 9 wherein the one or more functions are non-performance
critical functions.

14. The method of claim 13 wherein the non-performance critical functions are
selected from the group consisting of:

cache flushing, cache invalidation, setting processor features, reading processor
features, machine check handling, floating point calculations, processor diagnosis, Intel
32 bit architecture handling for backward compatibility, authentication, platform
management interrupt, diagnostic functions and debug functions.

15. A method of using firmware as microcode, the method comprising:
storing programmed code in firmware external to a processor;
executing, by the processor, the programmed code;

~~updating one or more registers associated with a logic unit on the processor in~~
response to the executing of the programmed code; and

controlling one or more functions of the logic unit on the processor based on a
value stored in the one or more registers.

16. The method of claim 15 further comprising controlling one or more functions of a
second logic unit on the processor based on a value stored in one of the registers
associated with the logic unit.

17. The method of claim 15 further comprising reprogramming the programmed code
in the firmware.

18. A processor comprising:
a plurality of logic units; and
one or more registers associated with each one of the plurality of logic units, the
one or more registers to trigger processor hardware logic functions when one of the
registers is updated in response to an external microcode instruction.

19. The processor of claim 18 wherein one or more of the registers are associated with
two or more of the logic units.

20. An article comprising:
a computer readable medium to store programmed code for use as microcode, the
~~computer readable medium to reside outside of a processor.~~

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